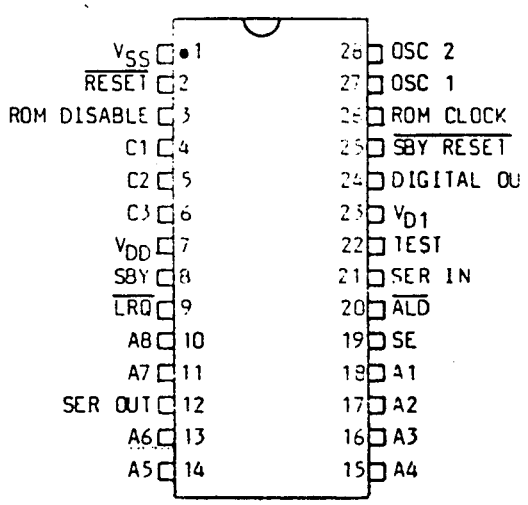
GENERAL INSTRUMENT	SPO256A

NARRATOR™ SPEECH PROCESSOR

FEATURES

- Natural Speech
- Stand Alone Operation with Inexpensive Support Components
- Wide Operating Voltage
- Word, Phrase, or Sentence Library, ROM Expandable
- Expandable to 491K of ROM Directly
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis; Formant Synthesis; and Allophone Synthesis

PIN CONFIGURATION
28 LEAD DUAL IN LINE
Top View



GENERAL DESCRIPTION

The SPO256A Speech Processor (SP) is a single chip N-Channel MOS LSI device that is able, using its stored program to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5KHz, a dynamic range of 42dB, and a signal to noise ratio of approximately 35dB.

The SPO256A incorporates four basic functions:

- A software programable digital filter that can be made to model a VOCAL TRACT.
- A 16K ROM which stores both data and instuctions (THE PROGRAM).
- A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word strings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

ALLOPHONE BASED SPEECH PROCESSOR - SPO256A-AL2

One example of a preprogramed SPO256A is the AL2 pattern.

The SPO256A-AL2 is available preprogramed with a standard ROM Pattern containing 64 allophones. Through the concatenation of selected allophones the user can construct any word in the English language, thereby providing an unlimited vocabulary.

A complete description of the SPO256A-AL2 is contained in the SPO256A-AL2 Data Sheet.

APPLICATIONS

- Telecommunications
- Appliances
- Computer Peripherals
- Automotive
- Personal Computers
- Toys/Games
- Educational Aids
- Warning Systems
- Security Systems
- Electronic Musical Instrum
- Aids to the Blind
- Narrow Bandwidth
- Communication Systems

OPERATION DESCRIPTION

The addressing of the SPO256A is controlled by the address pins (A1-A8). Address Load (ALD), and Strobe Enable (SE). Speech data for the SPO256A may be stored within the internal 16K ROM and/or an external serial speech ROM.

There are two modes available for loading an address into the chip. Strobe Enable (SE) controls which mode will be used.

Mode 0 (SE=0). The speech processor will latch an address when any one (or more) address pin makes a low to high transition. All address lines must be returned to the low state prior to entering a new address. (Note: Address zero (0000 0000) is not a valid address in this mode of operation.) In order to best utilize this mode of operation, a vocabulary should consist of no more than eight individual words or phrases such that single address line transitions can be made. These words or phrases must be stored using the following entry point address: 1, 2, 4, 8, 16, 32, 64 and 128.

NOTE: There is a 2 byte overhead penalty paid for each dummy entry point between the entry points actually used.

Mode 1 (SE=1). The SPO256A will latch an address using the ALD pin. The desired address is set up on the address bus (A1-A8) and then ALD is pulsed low. Any address can be loaded using this mode, but certain set up and hold times are required (refer to the timing diagrams for the specific times).

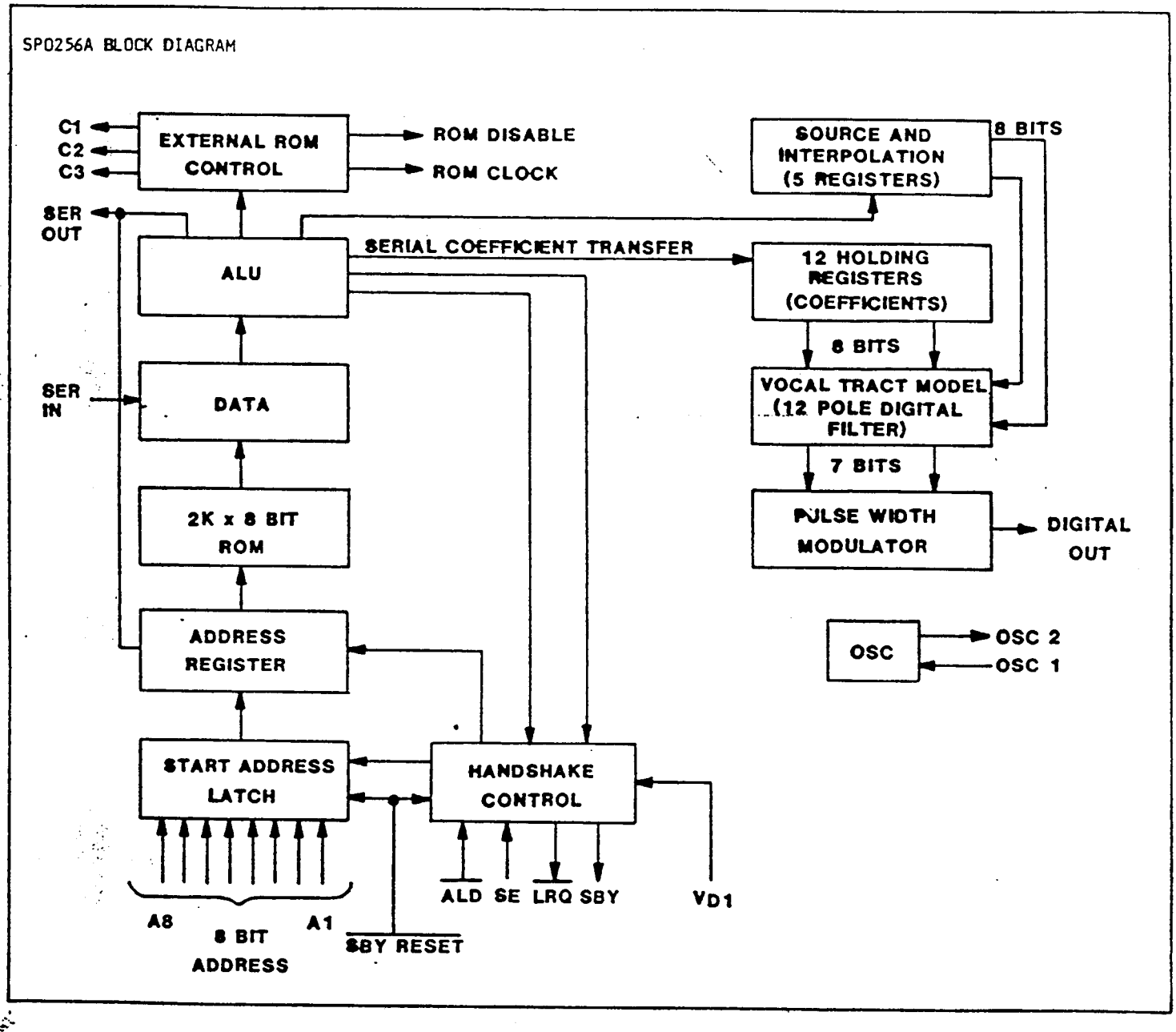
Two microprocessor interface pins are available for loading of addresses using mode 1. They are LRQ and SBY. Load Request (LRQ) tells the processor when the address input buffer is full. Standby (SBY) tells the processor that the chip has stopped talking and no new address has been loaded.

When LRQ is low, a new address may be loaded onto the address bus. Strobing ALD will cause the new address to be loaded and LRQ to go high. LRQ will return low when the address buffer is available to accept a new address. The SPO256A is capable of latching one new address while speaking the last utterance (word or phrase). The time between address load requests is variable, depending on the length of the utterance currently being spoken.

Standby (SBY) goes low when an address is loaded and will stay low until all internal instructions have been completed (i.e. the speech chip stops talking). If a second address has been loaded before the chip stops speaking the first utterance, SBY will stay low through the completion of the second utterance (ad infinitum).

The SPO256A may be partially powered down when SBY is high to conserve battery life, provided VDI remains powered. During power down and power up, reset should be held low to ensure the proper reset condition. While the speech processor is in the partial power down state, the handshake control signals (ALD, SE, LRQ, and SBY) and the address bus are active. However, the SPO256A will not output the addressed speech data until after V_{DD} is reapplied.

SP0256A BLOCK DIAGRAM



PIN FUNCTIONS

PIN NUMBER	NAME	FUNCTION
1	V_{SS}	Ground
2	$\overline{\text{RESET}}$	A logic 0 resets that portion of the SP powered by V_{DD}. Must be returned to logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM a logic 1 disables the external ROM.
4, 5, 6	C1, C2, C3	Output control lines for use with an external serial speech ROM. Refer to the SPR016 or SPR128 data sheet for details.
7	V_{DD}	Power supply for all portions of the SP except the microprocessor interface logic.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9	$\overline{\text{LRQ}}$	$\overline{\text{LOAD REQUEST}}$. $\overline{\text{LRQ}}$ is a logic 1 output whenever the input buffer is full. When LRQ goes to a logic 0, the input port may be loaded by placing the 8 address bits on A1-A8 and pulsing the ALD input.
10, 11, 13, 14, 15, 16, 17, 18	A8, A7, A6, A5 A4, A3, A2, A1	8 bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, ALD is disabled and the SP will automatically latch in the address on the input bus approximately 1us after detecting a logic 1 on any address line.
20	$\overline{\text{ALD}}$	$\overline{\text{ADDRESS LOAD}}$. A negative pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes LRQ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.

PIN FUNCTIONS (continued)

PIN NUMBER	NAME	FUNCTION
22	TEST	This pin should be grounded for normal operation.
23	VD1	Power supply for the microprocessor interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5KHz low pass filter and amplifier, will drive a loudspeaker.
25	$\overline{\text{SBY RESET}}$	STANDBY RESET. A logic 0 resets the microprocessor interface logic and the address latches. Must be returned to logic 1
26	ROM CLOCK	This is a 1.56MHz clock output used to drive an external serial speech ROM.
27	OSC1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC2	XTAL OUT. Output connection for a 3.12MHz crystal.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All pins with respect to V_{SS}..... -0.3 to 8.0V
Storage Temperature..... -25°C to 125°C

Standard Conditions

Clock - Crystal Frequency..... 3.120MHz
Operating Temperature..... T_A = 0°C to +70°C

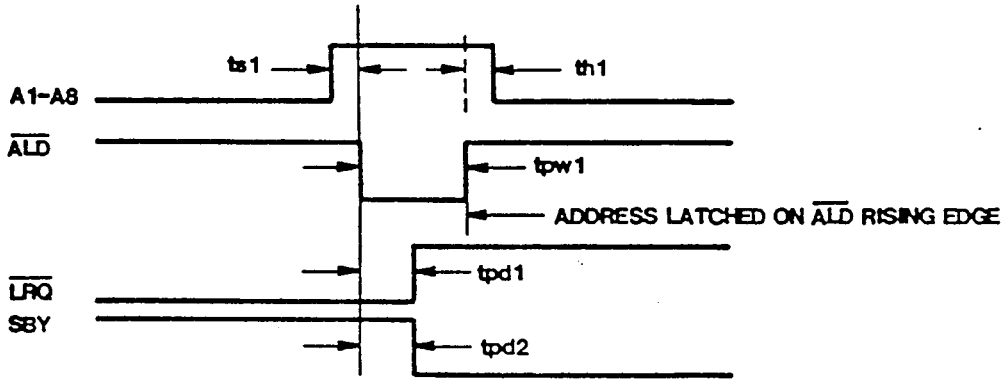
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

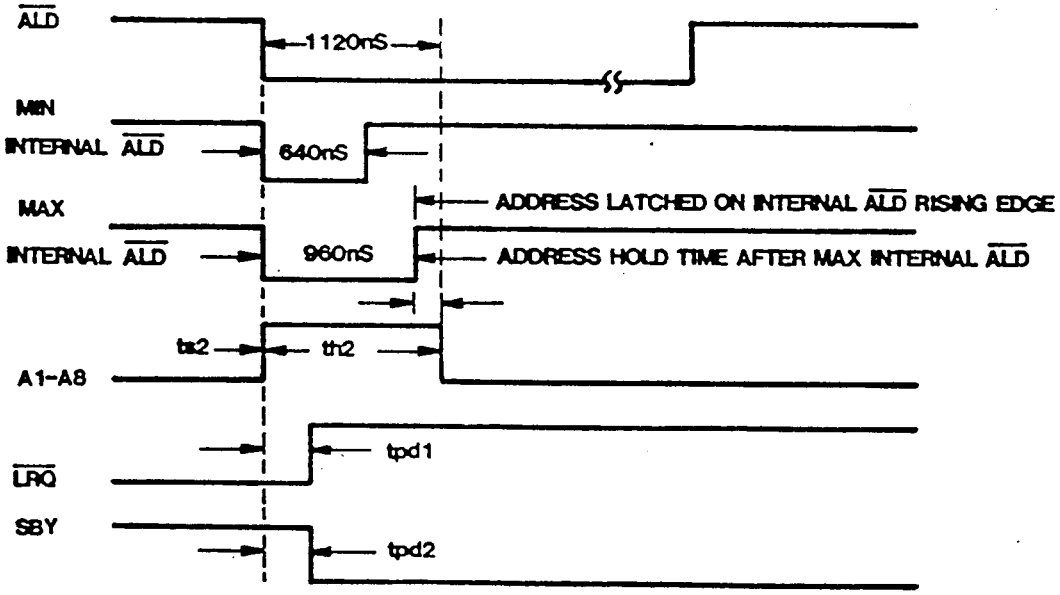
DC CHARACTERISTICS/SP0256A

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.6	-	7.0	V	
	V_{D1}	4.6	-	7.0	V	
Supply Current	I_{DD}	-	-	80	mA	25°C no loads. Reset and SBY. Reset high. OSC1=3.12MHz. All other inputs floating. 95mA MAX at 0°C
	I_{D1}	-	-	25	mA	25°C same as above 29.0mA MAX at 0°C
INPUTS						
A1-A8, $\overline{ALD}$, SERIN, TEST, SE						
LOGIC 0	V_{IL}	0.0	-	0.6	V	
LOGIC 1	V_{IH}	2.4	-	V_{D1}	V	
CAPACITANCE	C_{IN}	-	-	10	pf	0 volts bias, f=3.12 MHz
LEAKAGE	I_L	-	-	+10	ua	V_{PIN} = 7.0V Other Pins = 0.0V
$\overline{RESET}$, $\overline{SBY\ RESET}$						
LOGIC 0	V_{RSIL}	0.0	-	0.6	V	V_{RSIH} MIN at V_{D1}=4.6V
LOGIC 1	V_{RSIH}	4.0	-	V_{D1}	V	V_{RSIH} MIN increases by .2V per volt of V_{D1} increase
OUTPUTS						
$\overline{SBY}$, Digital Out, C1, C2, C3, $\overline{LRQ}$, ROM DIS, ROM CLK, SEROUT						
LOGIC 0	V_{OL}	0.0	-	0.6	V	I_{OL}=0.72ma (2LS TTL Loads)
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	I_{OH}=-50ua (2LS TTL Loads)
OSCILLATOR						
OSC 2 (Output)						When driven from external input.
LOGIC 0	V_{OL}	0.0	-	1.0	V	OSC1 (Input)=4.00V MIN at V_{D1}=4.60V
LOGIC 1	V_{OH}	2.5	-	V_{D1}	V	OSC1 (Input)=0.60V MAX

CHARACTERISTICS - AC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{ALD}$	t_{pw1}	200	-	960	ns	$200 \leq \overline{ALD} \leq 960$ ns
A1-A8 Set Up	t_{s1}	160	-	-	ns	
Hold	t_{h1}	160	-	-	ns	
$\overline{LRQ}$	t_{pd1}	-	-	300	ns	
SBY	t_{pd2}	-	-	300	ns	

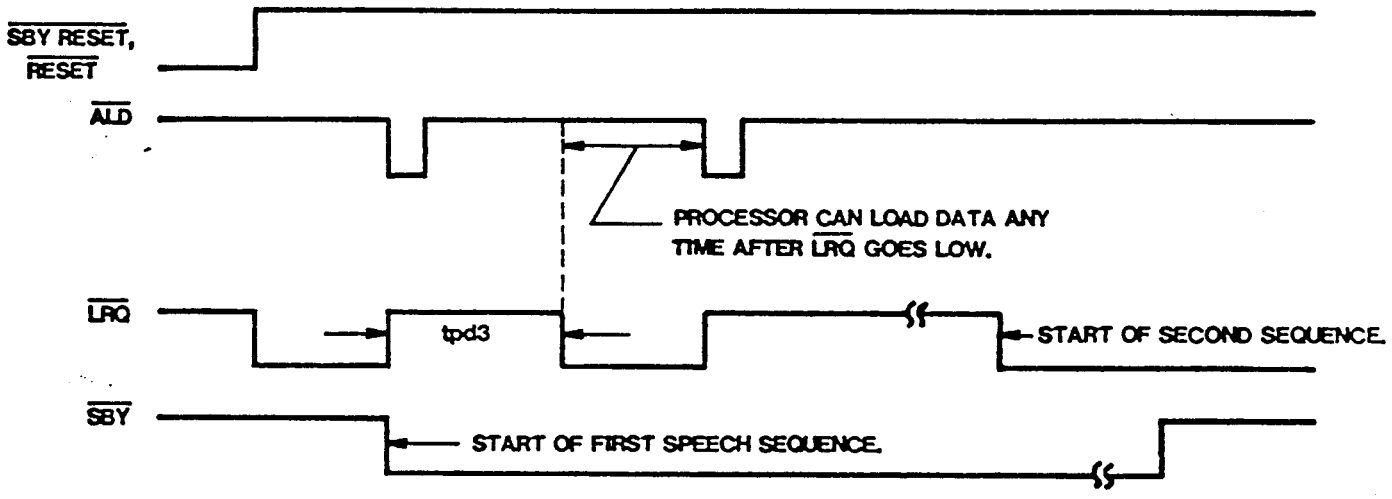


CHARACTERISTICS - AC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
A1-A8 Set Up	t_{s2}	0	-	-	ns	$\overline{ALD} > 960$ ns
Hold	t_{h2}	1120	-	-	ns	
$\overline{LRQ}$	t_{pd1}	-	-	300	ns	
SBY	t_{pd2}	-	-	300	ns	



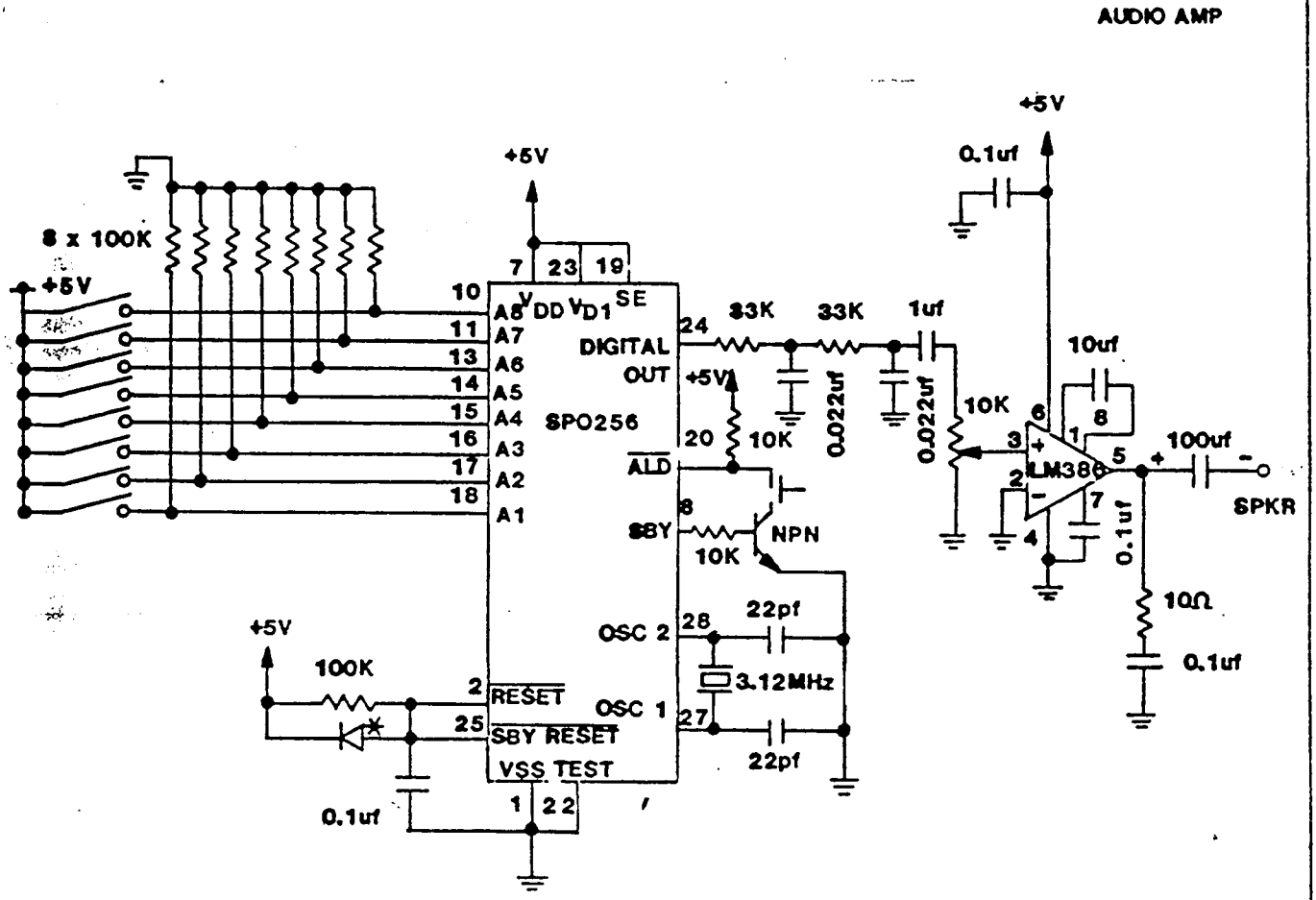
CHARACTERISTICS - AC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{LRQ}$	t_{pd3}	16.67	-	33.3	µS	Address Buffer ready for next load.

TYPICAL TIMING SEQUENCE



CHARACTERISTICS - AC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Clock	F	-	3.120	-	MHz	Crystal
Clock Duty Cycle	-	48	-	52	%	Osc., driven from
Reset, SBY Reset	t_{pw2}	25	-	-	µs	external

TYPICAL APPLICATION STAND ALONE CONFIGURATION



*Diode possibly necessary if power is turned off then on in less than 50 ms.

TYPICAL APPLICATION MICROCOMPUTER INTERFACE